T.J. Gabara 80

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Thaddeus J. Gabara
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Examiner: Hai L. Nguyen

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: Leura M. Hamla Date: November 26, 2003

Title: Comparator Circuits Having Non-Complementary Input Structures

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SUPPLEMENTAL APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Appeal Brief is submitted in response to the Office Action dated August 28, 2003 in the above-referenced application, in which the Examiner reopened prosecution in response to the Appeal Brief filed June 9, 2003.

Applicant has submitted concurrently herewith a response to the Office Action, requesting reinstatement of the appeal.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc. The assignee Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

STATUS OF CLAIMS

The present application was filed on May 30, 2001 with claims 1-41. Applicant filed a Response to Restriction Requirement on March 20, 2002, electing claims 1-7, 36, 37, 40 and 41 for prosecution on the merits. Claims 8-35, 38 and 39 were initially withdrawn from consideration in response to the election, and claims 40 and 41 were subsequently withdrawn from consideration in view of an Amendment filed by Applicant on September 25, 2002. Claims 1-7, 36 and 37 are therefore currently pending in the application.

Claims 1-7 and 36 stand rejected under 35 U.S.C. §102(b), and claim 37 stands rejected under 35 U.S.C. §103(a). Claims 1-7, 36 and 37 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF INVENTION

The present invention is directed to comparator circuits that are capable of comparing non-complementary input signals. With regard to independent claims 1, 36 and 37, each of these claims calls for a comparator circuit having an evaluation element and first and second input legs coupled thereto, with the first and second input legs being adapted to receive respective first and second input signals, and with the evaluation element <u>being adapted to perform a comparison of the first and second input signals</u>. Claims 1, 36 and 37 further specify that each of the first and second legs has "associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals." Claims 1 and 37 further specify that the first and second input legs have "non-complementary structures relative to one another." Claim 36 further specifies that the first and second input signals are "non-complementary input signals."

An example of an arrangement of the type claimed is shown in FIG. 11 of the drawings, and described as follows in the specification at page 15, line 7 to page 16, line 8, with emphasis supplied:

FIG. 11 shows a basic non-complementary comparator circuit in accordance with an illustrative embodiment of the invention. . . . The circuit includes a cross-coupled RAM cell formed of transistors m1, m2, m3 and m4. . . .

Inputs in_1 and in_2 are applied to evaluation legs denoted as R_1 and R_2 respectively. As previously noted, evaluation legs are also referred to herein as input legs. <u>In accordance with the invention, these legs have input structures which are non-complementary relative to one another, and therefore do not behave as conventional digital circuit structures</u>. The input legs are coupled to nodes of the RAM cell, e.g., nodes *out* and *outn* in this illustrative circuit. . . .

The evaluation legs in the basic comparator circuit of FIG. 11 are viewed as variable resistances during evaluation. More particularly, the variable resistance associated with left leg R_1 is a function of input in_1 and the variable resistance associated with right leg R_2 is a function of input in_2, as is shown in the figure. The outputs *out* and *outn* of the FIG. 11 comparator circuit are a function of the variable resistances as follows:

If ($R_1 < R_2$), the circuit will evaluate to *out* = 1 and *outn* = 0.
If ($R_1 > R_2$), the circuit will evaluate to *out* = 0 and *outn* = 1.

In this embodiment, the evaluation occurs when the clock signal ck goes low, although this is of course by way of example and not a requirement of the invention.

<u>The FIG. 11 comparator circuit by virtue of the variable resistances R_1 and R_2 is able to compare input signal in_1 against input signal in_2, even though in_1 may not be the complement of in_2</u>. In other words, if the binary weight of in_1 is greater than the binary weight of in_2, $R_1 < R_2$ and *out* = 1, thereby indicating that $in_1 > in_2$. <u>As noted previously, conventional comparators are generally unable to process non-complementary inputs in this manner</u>. The variable resistances may be implemented using weighted arrays of transistors, as will be described below.

The present invention as set forth in claims 1, 36 and 37 is thus directed to particularly advantageous comparator circuit arrangements that are capable of comparing non-complementary input signals. As noted above, conventional comparator circuits are unable to compare non-complementary input signals.

ISSUES PRESENTED FOR REVIEW

1. Whether claims 1-7 and 36 are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 5,901,087 (hereinafter "Pascucci").
2. Whether claim 37 is unpatentable under 35 U.S.C. §103(a) over Pascucci.

GROUPING OF CLAIMS

With regard to Issue 1, claims 1, 2, 4-7 and 36 stand or fall together, and claim 3 stands or falls alone.

With regard to Issue 2, claim 37 stands or falls alone.

ARGUMENT

Issue 1

Applicant respectfully traverses the §102(b) rejection.

With regard to independent claims 1 and 36, each of these claims calls for a comparator circuit having an evaluation element and first and second input legs coupled thereto, with the first and second input legs being adapted to receive respective first and second input signals, and with the evaluation element being adapted to perform a comparison of the first and second input signals. Claims 1 and 36 further specify that each of the first and second legs has "associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals." Claim 1 further specifies that the first and second input legs have "non-complementary structures relative to one another." Claim 36 further specifies that the first and second input signals are "non-complementary input signals."

As indicated previously herein, the present invention as set forth in claims 1 and 36 is directed to particularly advantageous comparator circuit arrangements that, unlike conventional comparator circuits, are capable of comparing non-complementary input signals.

Applicant respectfully submits that such arrangements are not taught or suggested by the Pascucci reference. More particularly, as will be described below, Pascucci fails to teach or suggest an arrangement in which an evaluation element is adapted to perform a comparison of first and second input signals applied to respective first and second input legs as claimed. Pascucci therefore fails to provide the significant advantages associated with the claimed arrangement in terms of its ability to compare non-complementary input signals.

Applicant notes that the Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicant submits that the Examiner has failed to establish anticipation of at least independent claims 1 and 36 by the Pascucci reference.

The Examiner in formulating the §102(b) rejection argues that the claimed evaluation element corresponds to virtual ground latch structure 2 of Pascucci FIG. 2, and that the claimed first and second input legs correspond to left and right circuitry coupled to respective nodes B and B′ in Pascucci FIG. 2. The Examiner further argues that the claimed first and second input signals correspond to buses YM<0-15> and YN<0-15> of Pascucci FIG. 2, described in column 3, lines 40-41, and that the claimed variable parameter values that are functions of the respective input signals correspond to current signals Il and Ir of Pascucci FIG. 2. See the Office Action dated August 28, 2003 at pages 2-3, section 3.

Applicant respectfully submits that if the claimed first and second input signals correspond to buses YM<0-15> and YN<0-15>, as alleged by the Examiner, then the arrangement shown in Pascucci FIG. 2 does not meet other limitations of the claims at issue. More specifically, with

reference to FIG. 2 of Pascucci, it can be seen that each of the left circuitry and the right circuitry associated with respective nodes B and B′ is coupled in substantially the same manner to both the YM<0-15> bus and the YN<0-15> bus. Therefore, neither the left circuitry nor the right circuitry will have associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, as required by the claim language. Also, if the Examiner believes that each of the claimed first and second input signals corresponds to the combination of the YM<0-15> bus and the YN<0-15> bus, then the evaluation element is not adapted to perform a comparison of the first and second input signals, as required by the claim language, since the combination of buses applied to both the left and right circuitry in this case is always the same.

Applicant further submits that the virtual ground latch structure 2, which the Examiner has characterized as corresponding to the claimed evaluation element, is not adapted to perform a comparison of any input signals that may be associated with the buses YM<0-15> and YN<0-15>. In other words, the buses YM<0-15> and YN<0-15> shown in Pascucci FIG. 2 are not compared by the virtual ground latch structure 2.

Moreover, there are no other input signals in Pascucci that are applied to respective first and second input legs and which are compared by the virtual ground latch structure 2. For example, as Applicant described in the Appeal Brief filed June 9, 2003, the Il and Ir current signals referred to in column 4, lines 52-56 of Pascucci cannot read on the claimed first and second input signals. As noted above, claims 1 and 36 call for first and second input legs adapted to receive respective first and second input signals, but the Il and Ir current signals are not input signals in the Pascucci device, in that these signals are not supplied as inputs to the Pascucci device. Instead, Il and Ir are simply used to identify currents flowing through the respective branches 8 and 9 associated with the respective nodes B and B′ in Pascucci FIG. 2.

Also as indicated previously, claims 1 and 36 further specify that each of the first and second legs has associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals. This limitation is clearly not met if one attempts to characterize the Il and Ir current signals as the claimed input signals, since there is no variable parameter in either branch 8 or 9 that is a function of the respective current signal Il or Ir. Thus, the

current signals Il and Ir cannot reasonably be characterized as the claimed input signals, without violating other requirements of the claim language.

Furthermore, Pascucci specifically teaches away from the claimed arrangement by indicating that the buses YM<0-15> and YN<0-15> collectively characterize a "selection means" which "provides the ability to select a memory cell from the memory cell matrix" comprising memory cells 16 and 17 (Pascucci, column 3, lines 34-43). The FIG. 2 circuit thus does not compare input signals associated with the buses YM<0-15> and YN<0-15>, but instead determines if particular ones of the memory cells 16 and 17 are programmed or unprogrammed (Pascucci, column 5, line 39 to column 6, line 3).

Pascucci therefore fails to teach or suggest at least the limitation of claims 1 and 36 regarding an evaluation element of a comparator circuit being adapted to perform a comparison of first and second input signals applied to respective first and second input legs. Pascucci thus fails to teach or suggest "each and every element" of claims 1 and 36 in "as complete detail" as is contained in those claims. The §102(b) rejection is therefore believed to be improper, and should be withdrawn.

Dependent claims 2-7 are believed allowable for at least the reasons identified above with regard to their corresponding independent claim 1. Moreover, one or more of these claims are believed to define separately-patentable subject matter relative to Pascucci and the other art of record.

With regard to dependent claim 3, this claim specifies that the "variable parameter having a value that is a function of a corresponding one of the input signals" comprises a variable resistance. An example is the variable resistance $R_1 = F(in_1)$ or $R_2 = F(in_2)$ as described previously herein in conjunction with FIG. 11 of the drawings. Applicant notes that the Examiner has failed to identify with any specificity the particular teachings from Pascucci that are alleged to meet this variable resistance limitation. Applicant respectfully submits that there is no such variable resistance, having a value which is a function of an input signal, associated with either of the branches 8 or 9 in Pascucci. Dependent claim 3 is therefore not anticipated by Pascucci.

Issue 2

Independent claim 37 includes limitations similar to those of claim 1, and is therefore believed allowable for at least the reasons identified above with regard to claim 1. The arguments presented above with regard to independent claim 1 are therefore realleged and incorporated herein by reference. Since Pascucci fails to teach or suggest all of the limitations of claim 37, the §103(a) rejection is also believed to be improper, and should be withdrawn.

In view of the above, Applicant believes that claims 1-7, 36 and 37 are in condition for allowance, and respectfully requests withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,

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APPENDIX

1. A comparator circuit comprising:

an evaluation element; and

at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs having non-complementary structures relative to one another and being adapted to receive respective first and second input signals, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of the first and second input signals.

2. The comparator circuit of claim 1 wherein the first and second input signals comprise non-complementary input signals.

3. The circuit of claim 1 wherein the variable parameter for a given one of the input legs comprises a variable resistance.

4. The comparator circuit of claim 1 wherein the variable parameter for a given one of the input legs comprises a variable current.

5. The comparator circuit of claim 1 wherein the variable parameter for a given one of the input legs comprises a variable voltage.

6. The comparator circuit of claim 1 wherein the evaluation element comprises a memory cell.

7. The comparator circuit of claim 6 wherein the evaluation element comprises a random access memory (RAM) cell.

8. The comparator circuit of claim 1 wherein the evaluation element comprises a differential amplifier.

9. The comparator circuit of claim 1 wherein at least one of the first and second input legs comprises a weighted array of transistors, each of the transistors in the weighted array adapted to receive a particular portion of an input signal applied to that leg.

10. The comparator circuit of claim 9 wherein the weighted array comprises an array of transistors digitally sized in width in accordance with a corresponding relationship between portions of a digital input signal.

11. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, and wherein the first and second inputs each comprise a digital word having a plurality of bits, and wherein each transistor of the associated weighted array of transistors is adapted to receive as an input a corresponding bit of a given one of the digital words.

12. The comparator circuit of claim 11 wherein the transistors of the weighted array are weighted in accordance with factors $2^0, 2^1, \ldots 2^{n-1}$ in width and the weighted array is adapted to receive a corresponding input signal comprising an n-bit digital word.

13. The comparator circuit of claim 9 wherein the weighted array comprises an additional transistor having an input adapted to receive an offset signal, the offset signal being configured so as to ensure a predictable output result if comparison of the first and second inputs would otherwise result in an unpredictable output.

14. The comparator circuit of claim 1 being implemented in a pipelined structure, the first and second input legs each being adapted to receive multi-bit digital words as the respective first and second input signals, the pipelined structure having a plurality of stages with each stage involving a comparison of designated portions of the multi-bit digital words.

15. The comparator circuit of claim 14 wherein the first and second input legs are adapted to receive $m \times n$-bit digital words, and the pipelined structure has m stages with each stage configured to perform an n-bit comparison of a selected portion of the digital words.

16. The comparator circuit of claim 14 wherein the pipelined structure comprises an N-tree to N-tree structure.

17. The comparator circuit of claim 14 wherein the pipelined structure comprises an N-tree to P-tree structure.

18. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, the first and second input signals each comprising a digital word having a plurality of bits, wherein each transistor of a given one of the weighted arrays is adapted to receive as an input a corresponding bit of a given one of the digital words, each of the transistors in each of the weighted arrays having a substantially equal width such that comparison of the digital words implements a majority rule function.

19. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, the first and second input signals each comprising one or more balanced analog input signal pairs, inputs of parallel transistors in a particular one of the weighted arrays being adapted to receive respective signals of a given one of the pairs, each of the transistors in each of the weighted arrays having a substantially equal width such that the comparator circuit is configured to provide an analog common mode comparison.

20. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, the first and second input signals each comprising one or more analog input signals, inputs of parallel transistors in a particular one of the weighted arrays being adapted to receive corresponding ones of the analog input signals, each of the transistors in each of the

weighted arrays having a substantially equal width such that the comparator circuit is configured to provide an analog common mode comparison.

21. The comparator circuit of claim 1 being a first comparator circuit coupled with a second comparator circuit having an evaluation element and at least first and second input legs each coupled to a corresponding one of a first node and a second node of the evaluation element of the second comparator circuit, the first input leg of the first comparator being adapted to receive an input signal representing a first bound, the second input leg of the second comparator being adapted to receive an input signal representing a second bound, the second input leg of the first comparator and the first input leg of the second comparator both being adapted to receive another input signal, the first and second comparator circuits collectively being adapted to generate an output indicative of whether or not the other input signal falls within the first and second bounds.

22. The comparator circuit of claim 1 having at least a third input leg coupled to the first node of the evaluation element adjacent the first input leg, the third input leg having associated therewith a variable parameter having a value that is a function of a corresponding input signal, the evaluation element being adapted to perform a comparison of the result of an addition of at least first and third inputs applied to the respective first and third input legs with a second input applied to the second input leg.

23. The comparator circuit of claim 1 having a first plurality of input legs including the first leg coupled to the first node of the evaluation element, and a second plurality of input legs including the

second input leg coupled to the second node of the evaluation element, each of the input legs having associated therewith a variable parameter having a value that is a function of a corresponding input signal, the evaluation element being adapted to perform a comparison of the result of an addition of a first plurality of inputs applied to respective ones of the first plurality of input legs with the result of an addition of a second plurality of inputs applied to respective ones of the second plurality of input legs.

24. The comparator circuit of claim 22 being implemented as a serial adder-binary search (SA-BS) circuit having a finite state machine being adapted to generate inputs for application to the second input leg in accordance with a binary search process, so as to determine the result of an addition of inputs applied to the first and third input legs.

25. The comparator circuit of claim 24 wherein the SA-BS circuit is one of m SA-BS circuits each being adapted to perform an n-bit function so as to implement an m×n-bit serial adder.

26. The comparator circuit of claim 1 wherein a first set of input legs associated with the first node of the evaluation element and a second set of input legs associated with the second node of the evaluation element are adapted to receive a substantially constant current, for at least a designated period of time, so as to implement an analog adder function.

27. The comparator circuit of claim 23 further comprising a multiplexer being adapted to select a particular pair of the inputs for propagation to an output thereof so as to implement an add-compare-select (ACS) function.

28. The comparator circuit of claim 23 being one of a plurality of ACS circuits, each being adapted to compare at least a first pair of inputs with a second pair of inputs, the plurality of ACS circuits being implemented in a layered architecture having a plurality of layers including a final layer having a single one of the ACS circuits, the layered architecture being adapted such that winning pairs from one layer are compared against one another at a subsequent layer until a final winning pair is identified.

29. The comparator circuit of claim 28 further comprising an associated adder being adapted to perform an addition of the final winning pair of inputs.

30. The comparator circuit of claim 1 being a first comparator circuit and further comprising at least a second comparator circuit coupled in parallel therewith so as to implement a coupled memory cell comparator.

31. The comparator circuit of claim 30 further comprising a third comparator circuit having first and second input legs each coupled to a corresponding one of a first and second input leg of one of the first comparator circuit and the second comparator circuit.

32. The comparator circuit of claim 1 wherein the first and second input legs each have associated therewith a plurality of mask inputs, the mask inputs being adapted to receive mask signals operative to configure the first and second input legs so as to implement a masking of corresponding portions of the first and second input signals from consideration in the comparison performed by the evaluation element.

33. The comparator circuit of claim 1 wherein the first and second input legs each comprise a plurality of variable resistances arranged in a stack, each of the variable resistances having an input associated therewith, and the evaluation element comprises a differential amplifier.

34. The comparator circuit of claim 1 wherein at least one of the first and second input legs includes an offset signal input, the offset signal input being adapted to introduce signal information into the comparator circuit.

35. The comparator circuit of claim 34 wherein the signal information comprises carry input signal information.

36. A comparator circuit comprising:

an evaluation element; and

at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs being adapted to receive respective first and second non-complementary input signals, each of the first and second input legs

having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of the first and second input signals.

37. An integrated circuit comprising:

at least one comparator circuit, the comparator circuit comprising an evaluation element, and at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs having non-complementary structures relative to one another and being adapted to receive respective first and second input signals, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of first and second input signals.

38. A comparator circuit comprising:

an evaluation element; and

at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs being adapted to receive respective first and second input signals, each of the first and second input legs having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of the first and second input signals, wherein outputs of the comparator circuit are isolated from corresponding output nodes of

the evaluation element such that the comparison is substantially independent of asymmetry associated with the outputs of the comparator circuit.

39. A comparator circuit comprising:

a plurality of add-compare-select (ACS) circuits implemented in a layered architecture having a plurality of layers including a final layer having a single one of the ACS circuits and an associated adder being adapted to perform an addition of a final winning pair of inputs, the layered architecture being configured such that winning pairs from one layer are compared against one another at a subsequent layer until the final winning pair is identified.

40. (Amended) A circuit comprising at least first and second input legs, the first and second input legs having non-complementary structures relative to one another, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding input signal, a difference in the variable parameters associated with the first and second input legs being detectable in the circuit;

wherein at least one of the first and second input legs comprises a weighted array of transistors, each of the transistors in the weighted array adapted to receive a particular portion of an input signal applied to that leg.

41. The circuit of claim 40 further comprising an evaluation element, wherein the first and second input legs are each coupled to a corresponding one of a first and second node of the evaluation

element, the evaluation element being adapted to perform a comparison of first and second input signals applied to the respective first and second input legs.